

PTO/SB/08A (10-01)
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Substitute for form 1449A/PTO				Complete if Known	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (use as many sheets as necessary)				Application / C nt. N .	Unknown /
				Filing Dat	March 01, 2002
				First Nam d Inventor	Paul T. Sasaki
				Art Unit	Unknown
				Examiner Name	Unknown
				Attorney Docket Number	X-1049 US
Sheet	1	of	1	10/090519 10/090519 10/090519	

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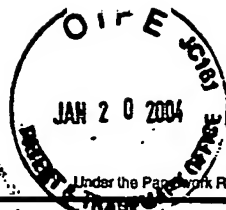
Examiner Signature	<i>John J. Jabore, Jr.</i>	Date Considered	<i>10/19/04</i>
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*EXAMINER: Initially reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

¹ Applicant's unique citation designation number (optional). ² See Kinds of USPTO Patent Documents at www.uspto.gov or MPEP 901.04. ³ Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). ⁴ For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. ⁵ Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST. 16 if possible. ⁶ Applicant is to place a check mark here if English language Translation is attached.

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Sheet 1 of 7

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Applicant's Cnf. No.	10/090,519 / 6632
Filing Date	March 01, 2002
First Name of Inventor	Paul T. Sasaki
Art Unit	2661
Examiner Name	Unknown
Attorney Docket Number	X-1049 US

U.S. PATENT DOCUMENTS

Examiner Initials *	Cite No.¹	Document Number		Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number - Kind Code (if known)				
JES		US-	4,758,985	07-19-88	Carter	RECEIVED JAN 22 2004 Technology Center 2600
		US-	5,142,625	08-25-92	Nakai	
		US-	4,855,669	08-08-89	Mahoney	
		US-	34,363	08-31-93	Freeman	
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		US-	5,274,570	12-28-93	Izumi et al.	
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		US-	5,574,930	11-12-96	Halverson Jr., et al.	

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		Country Code *	Number * Kind Code * (if known)				
JES		EP	0315275 A2	10-05-89	LSI Logic		
		WO	93 25968 A1	12-23-93	Furtek		
		EP	0 905 906 A2	03-31-99	Lucent		
		EP	1 235 351 A1	08-28-02	Matsushita Electric		

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John J. Fabone, Jr.

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		Art Unit	2661		
		Examiner Name	Unknown		
Sheet	2	of	7	Attorney Docket Number	X-1049 US

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OTHER - NON PATENT LITERATURE DOCUMENTS			
Examiner Initials *	Cite No ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
JJ		SAYFE KIAEI et al., "VLSI DESIGN OF DYNAMICALLY RECONFIGURABLE ARRAY PROCESSOR-DRAP," IEEE, February 1989, pp. 2484-2488, V3.6, IEEE, 3 Park Avenue, 17th Floor, New York, NY 10016-5997	
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Examiner Signature	<i>John J. Salome, Jr.</i>	Date Considered	10/19/04
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

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

First Named Inventor	Paul T. Sasaki
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Art Unit	2661
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Examiner Name	Unknown
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Attorney Docket Number	X-1049 US
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U.S. PATENT DOCUMENTS

Examiner Initials	Cite No.'	Document Number	Publication Date	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number - Kind Code (if known)	MM-DD-YYYY		
		US- 5,473,267	12-05-95	Stansfield	<div>RECEIVED</div> <div>JAN 22 2004</div> <div>Technology Center 260</div>
		US- 5,742,180	04-21-98	DeHon et al.	
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		US- 5,543,640	08-06-96	Sutherland et al.	
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		US- 5,933,023	08-03-99	Young	
		US- 09/991,412	11-16-01	Herron et al.	
		US- 6,389,558	05-14-02	Herrmann et al.	
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**Examiner
Signature**

John J. Tabone, Jr.

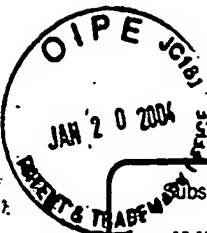
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			Filing Date	March 01, 2002	
			First Named Inventor	Paul T. Sasaki	
			Art Unit	2661	
			Examiner Name	Unknown	
Sheet	4	of	7	Attorney Docket Number	X-1049 US

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OTHER - NON PATENT LITERATURE DOCUMENTS			
Examiner Initials *	Cite No ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
JJS		XILINX, INC., "THE PROGRAMMABLE LOGIC DATA BOOK," 1994, Revised 1995, Xilinx, Inc., 2100 Logic Drive, San Jose, CA. 95124.	
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		RALPH D. WITTIG et al., "ONECHIP: AN FPGA PROCESSOR WITH RECONFIGURABLE LOGIC," April 17, 1996, pp 126-136, IEEE, 3 Park Avenue, 17th Floor, New York, NY 10016-5997	
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		WILLIAM B. ANDREW et al., "A FIELD PROGRAMMABLE SYSTEM CHIP WHICH COMBINES FPGA & ASIC CIRCUITRY," IEEE, May 16, 1999, pp. 183-186, IEEE, 3 Park Avenue, 17th Floor, New York, NY 10016-5997	
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Examiner Signature	<i>John J. Tabone, Jr.</i>	Date Considered	10/19/04
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				First Name of Inventor	Paul T. Sasaki
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				Examiner Name	Unknown
Sheet	5	of	7	Attorney Docket Number	X-1049 US

U.S. PATENT DOCUMENTS					
Examiner Initials *	Cite No. *	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number - Kind Code (if known)			
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		US- 09/991,410	11-16-01	Herron et al.	
		US- 09/968,446	11-16-01	Herron et al.	
		US- 5,760,607	06-02-98	Leeds et al.	RECEIVED
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		US- 6,163,166	12-19-00	Bielby et al.	
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Attorney Docket Number	X-1049 US

(use as many sheets as necessary)

Sheet	6	of	7
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**Examiner
Signature**

John J. Talbot, Jr.

Date Considered

10/19/84

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JJS		US- 6,519,753	02-11-03	Ang	
		US- 6,434,735	08-13-02	Watkins	
		US- 6,588,006	07-01-03	Watkins	
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		US- 6,242,945	06-05-01	New	
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Examiner Signature	<i>John J. Fabore, Jr.</i>	Date Considered	10/19/04
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